Body Bias Optimization for Variable Pipelined CGRA

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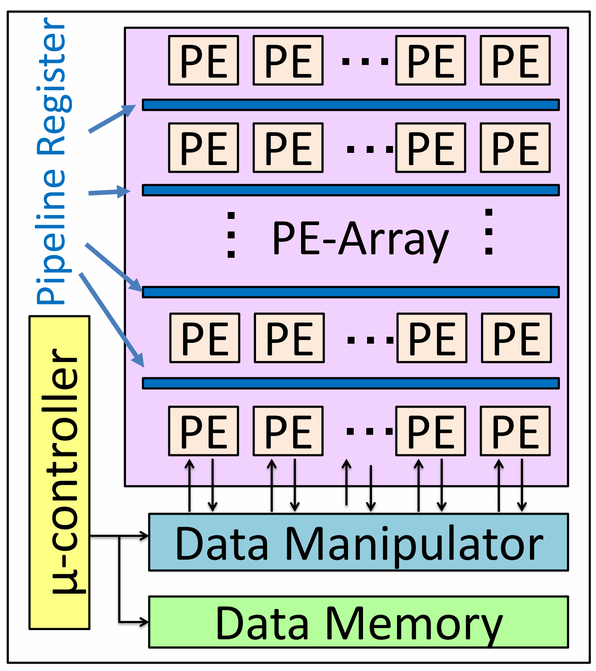
Introduction

VPCMA [1] is a CGRA (Coarse Grained Reconfigurable Architecture) providing a variable pipeline structure in its PE array. Also, it is implemented with the SOTB technology. The pipeline structure and body bias voltage can be changed in order to blance its performance and power consumption. In this work, we propose an optimization method for pipelined CGRA including VPCMA.

VPCMA (Variable Pipelined Cool Mega Array)

Architecture



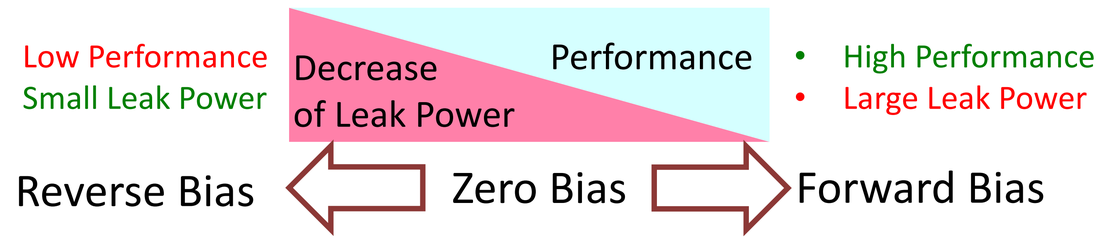
VPCMA diagram

- PE (Processing Element)
  - Power reduction
  - No register file
  - No clock tree
  - No dynamic reconfiguration
- Pipeline Register
  - Selection upon use
  - Variable pipeline structure
- PE Array
  - 12 cols × 8 rows of PEs
  - 7 pipeline registers

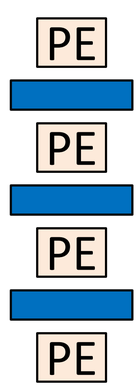
- Row level body bias control
  - Each PE row is supplied independent body bias voltage.
  - Balance of the delay time of each pipeline stage
    - Decreasing the delay time of the critical path
    - Increasing the delay time of the other paths
    - More power reduction

Complex Trade-off

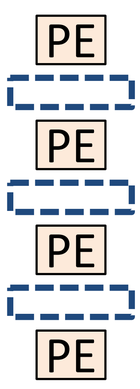
- Body bias voltage



- Pipeline structure



Large	Number of pipeline stage	Small
↗	Dynamic power of registers and clock	↘
↘	Dynamic power of glitches	↗
High	Performance	Low



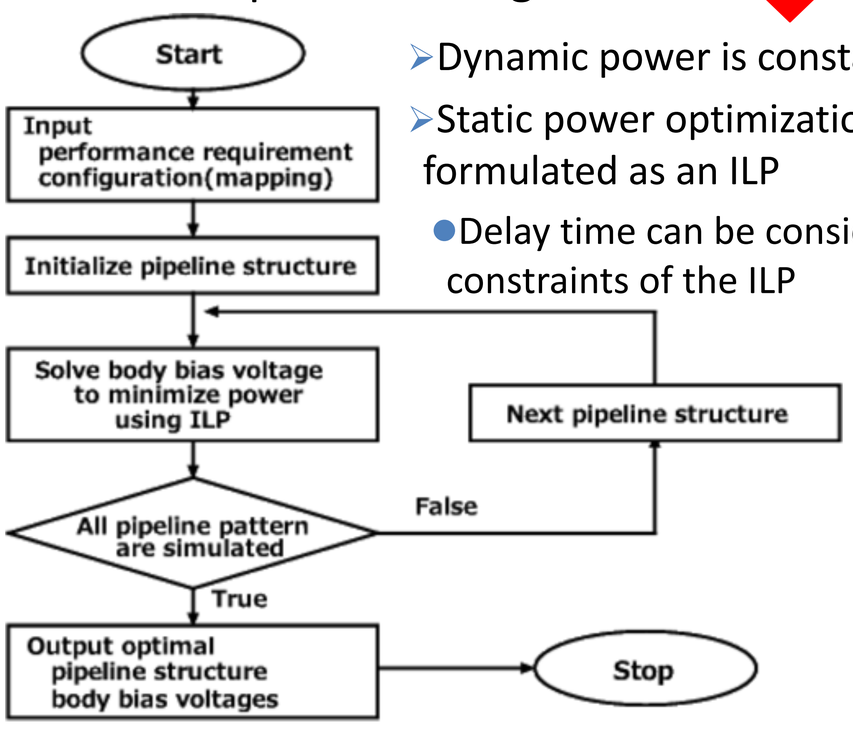
- Combination of pipeline structure and body bias control
  - Body bias voltage: 13 values (-2.0, -1.8, -1.6, ..., 0.4 V)
  - Pipeline structure: 128 patterns (2^7)
  - 13^8 × 128 possible solutions

Optimization Method

Optimization Flow with ILP (Integer Linear Program)

- Dependencies of each criteria
  - Static power
    - Depends on body bias voltage
    - Linear function
  - Delay time (Performance)
    - Depends on body bias voltage , mapping & pipeline structure
  - Dynamic power
    - Depends on delay time & pipeline structure

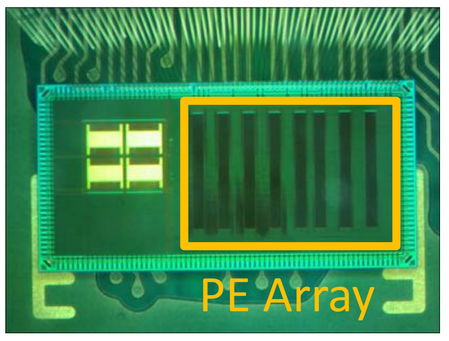
When pipeline structure is fixed and performance requirement is given



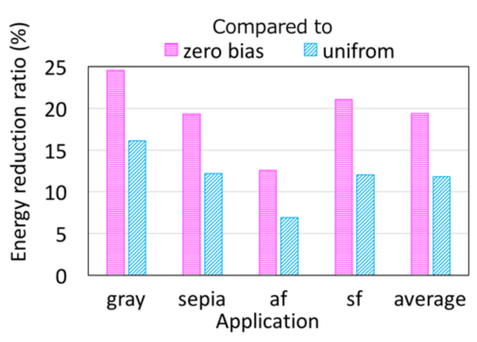
- Dynamic power is constant
- Static power optimization can be formulated as an ILP
  - Delay time can be considered to be constraints of the ILP

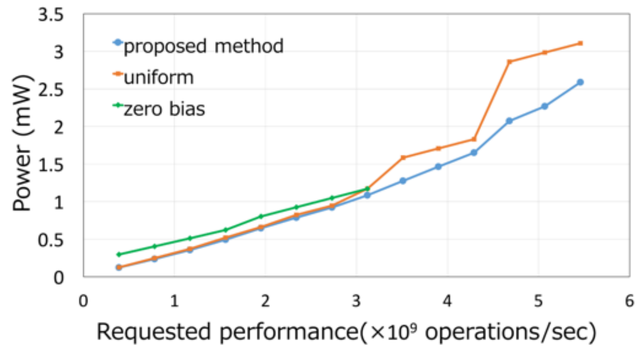
Results of Simulation

- Simulations
  - 4 image process application programs
    - gray, sepia, af, sf
  - Based on a real chip implementation
  - Fixed mapping



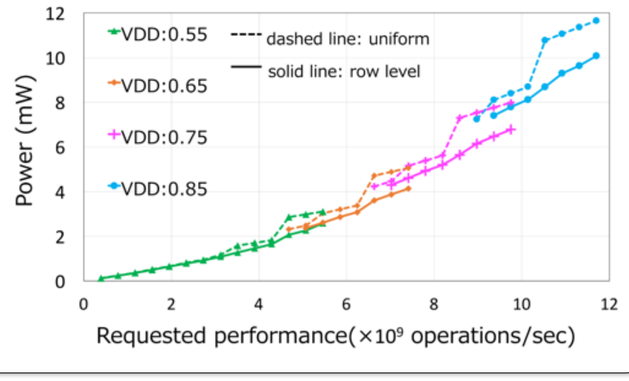
- Comparison with other body bias control methods





- Other control policies
  - Zero bias: no control of body bias
  - Uniform: whole PE array supplied with the same body bias
- Using body bias control
  - Extends performance limitation
- Using proposed method
  - Limited increase of power

- Comparison with VDD control
  - Suitable control for high performance
  - Uniform
    - Using VDD control is better
  - Proposed method
    - Using Body bias control is better



[1] N. Ando, K. Masuyama, H. Okuhara, and H. Amano, “Vari- able pipeline structure for coarse grained reconfigurable array cma,” in *2016 INTERNATIONAL CONFERENCE ON FIELD- PROGRAMMABLE TECHNOLOGY*, 2016, pp. 231–238.