Configuration Data Multicasting Method for Coarse-Grained Reconfigurable Architectures

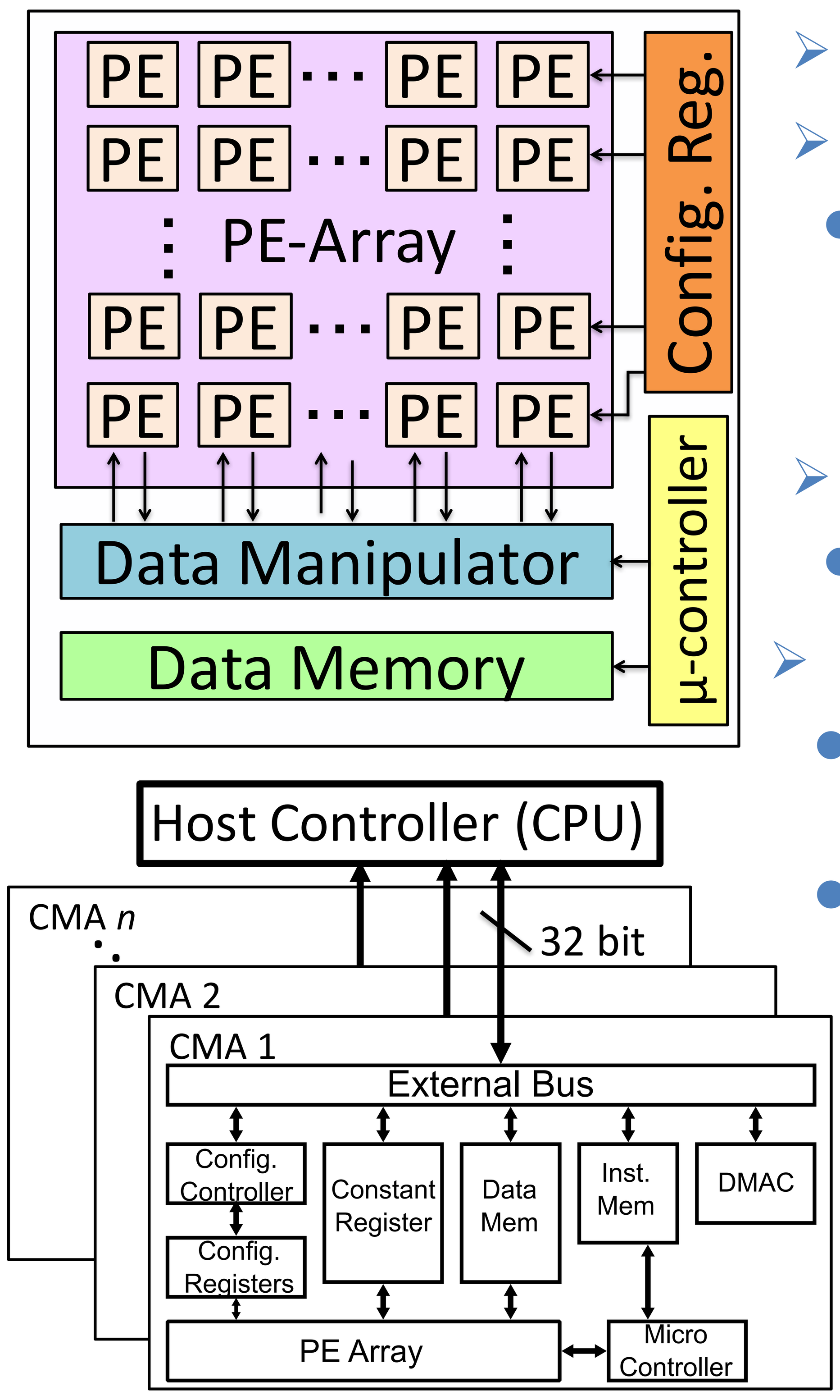
Takuya Kojima and Hideharu Amano, Keio University, Japan

Introduction

In CGRAs (Coarse-Grained Reconfigurable Architectures), its configuration time is sometimes an obstacle for efficient computing. In this work, we propose a novel configuration data compression technique based on a multicast configuration scheme called RoMultiC. In addition, two types of scheduling algorithms for the proposed technique are also proposed. Experimental results show that the proposed method achieves power reduction as well as reduced configuration.

Configuration Multicasting

CGRA Architecture



Entire system overview

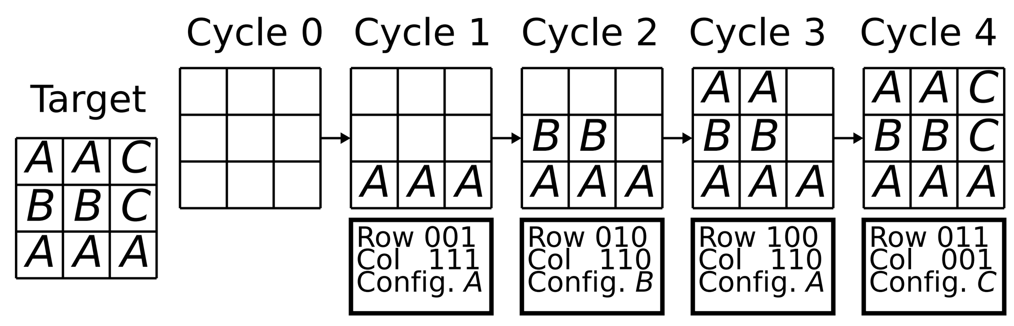
- CMA (Cool Mega Array) [1]
- PE (Processing Element)
  - Composed of
    1. Simple ALU
    2. Switching Element (SE)
- PE Array
  - 12 cols × 8 rows of PEs
- For a scalable system
  - Multiple CMA chips can be connected with a host CPU
  - Each component for each chip is mapped to same address space as the host CPU

Configuration data is transfered via a general purpse data bus

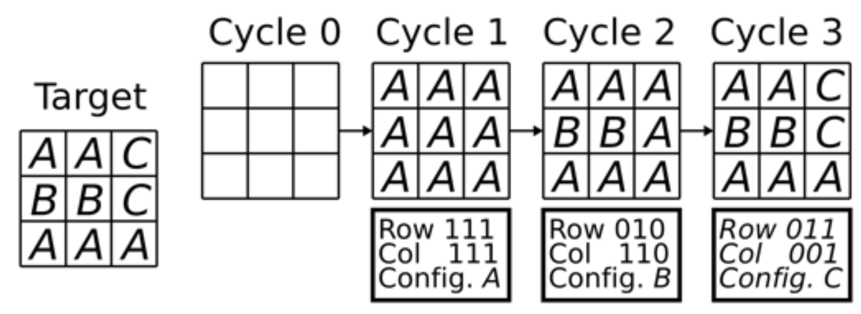
Configuration time is a concern

Multicasting Scheme

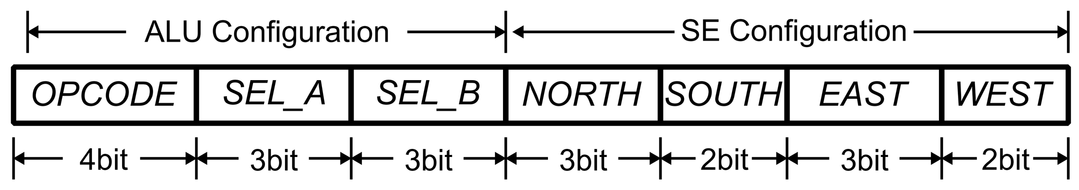
- RoMultiC [2]
  - Multicasting data to PEs which have the same config.
  - Using two bit-maps for PE rows & columns



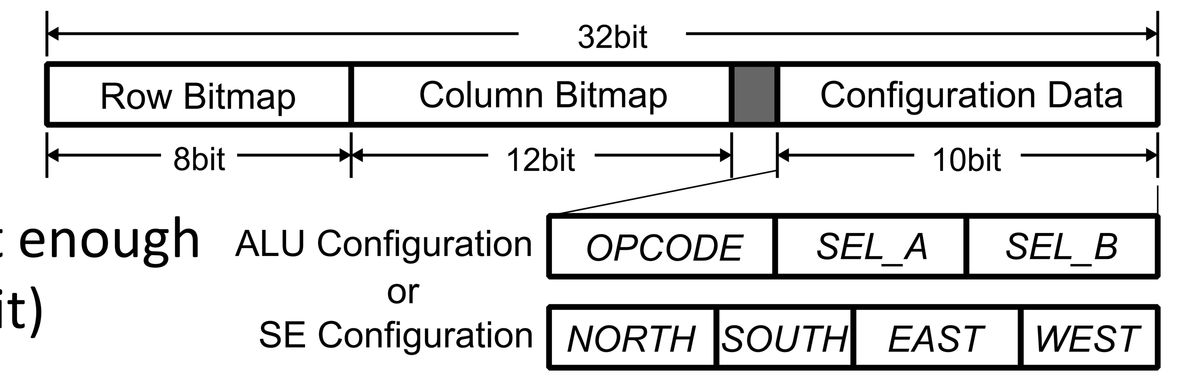
- Overwriting Scheduling
  - Possible to reduce more data
  - High priority to multicasting widely distributed configs.



- Configuration data format (20bit)



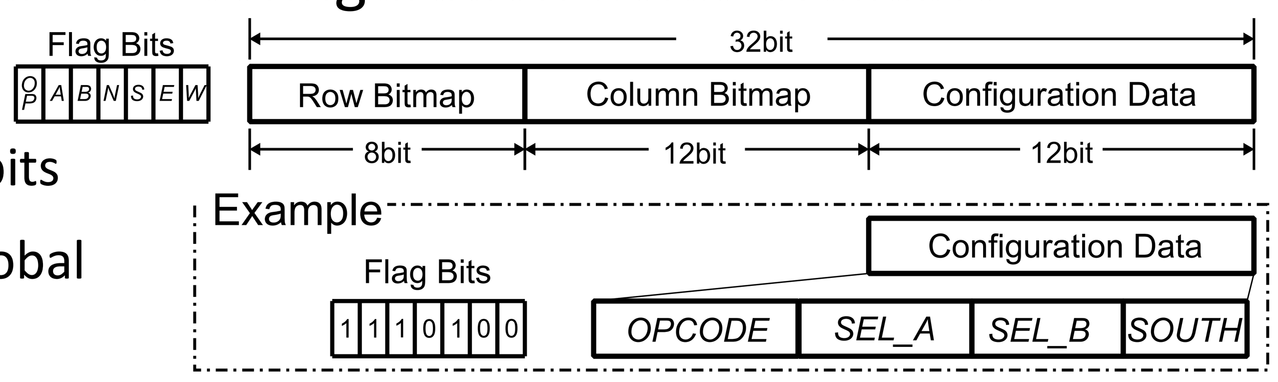
- 2 types of multicasting in the original CMA
  1. ALU-by-ALU
  2. SE-by-SE
  - Because of not enough data space (12bit)
  - Unused 2 bits space
  - Multicasted ALUs or SEs must have a completely same config.
    - Less possibility of data reduction for complex config.



Proposed Method

Fine-grain Multicasting

- Any combination of configuration fields available
  - Need for additional flag bits
  - Mapped to global address space



2. FGM-I: Integer-linear-program-based Fine-Grain Multicasting

- Guarantee of optimality but taking much time

$$\max S = \sum_i \sum_j \sum_k S_{ijk} * isFields_i * isRow_j * isCol_k$$

subject to

$$\sum_i bit\_width_i * isFields_i \leq bit\_width_{max}$$

If i-th field of the PE in the j-th row and k-th column is already fixed

$$isFields_i \cup isRow_j \cup isCol_k = 0$$

Scheduling Algorithms

- Greedy Scheduling
  - In order of largest multicasted configuration data
- How to find configuration patterns
  1. FGM-E: Espresso-based Fine-Grain Multicasting
     - Not always optimal but fast algorithm
     - Using a heuristic logic minimization algorithm: *Espresso*
       - Supporting ***Don't Care X*** as well as ***1*** and ***0***
     - For each unfixed configuration, making a truth table
       - Logic **0**: already fixed parts (to prevent them from being overwritten)
       - Logic **1**: same config. parts
       - Don't care ***X***: others

row	col	value
0	3	0
3	3	0
0	0	1
1	0	1
1	1	1
2	1	1
2	3	1
others		X

Truth Table associated with config. *B* after config. *A*s are fixed

			A
	B		*B*
B	*B*		
B			*A*

Target configuration (*A*s are fixed)

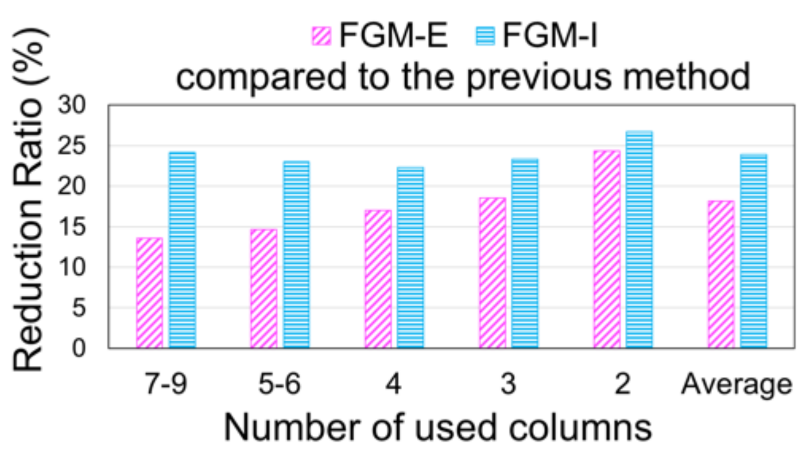
	0	1	3	2
0	1	X	0	X
1	1	1	X	X
3	X	0	X	X
2	X	1	1	X

Karnaugh map

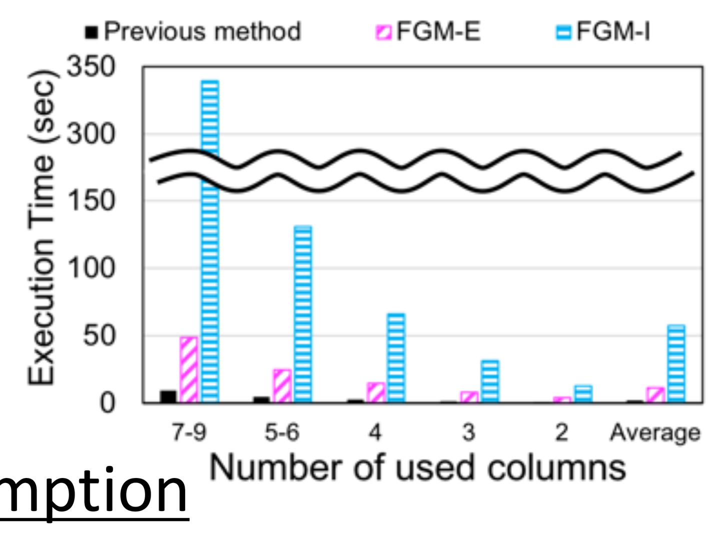
The largest circle is chosen

Evaluation

- Reduction Ratio
  - For randomly generated configs.
    - FGM-I is better for large configs.
    - FGM-I achieves around 20 % reduction regardless of the size
  - For config. of image process apps.
    - FGM-E: 11.7% , FGM-I: 19.14% (Avg.)



- Execution time
  - FGM-I takes quite a long time
  - FGM-E is finished within 1 min for any size of the configuration



- Area Overhead and Power consumption
  - The proposed method can be implemented with a negligible area overhead
  - It can reduce the dynamic power thanks to minimum overwriting

Area overhead of the configuration controller

	Area (mm²)	Overhead (%)
Previous method	0.944	—
Proposed method	1.04	9.76

Power comparison between both methods

	Dynamic (μW)	Static (μW)
previous method	514.5	6.125
Proposed method	329.3	6.247

[1] N. Ozaki, Y. Yasuda, M. Izawa, Y. Saito, D. Ikebuchi, H. Amano, H. Nakamura, K. Usami, M. Namiki, and M. Kondo, "Cool Mega-Arrays: Ultralow-Power Reconfigurable Accelerator Chips," *IEEE Micro*, vol. 31, no. 6, pp. 6–18, Nov 2011.

[2] S. Tsutsumi, V. Tunbunheng, Y. Hasegawa, A. Parimala, T. Nakamura, T. Nishimura, and H. Amano, "Overwrite configuration technique in multicast configuration scheme for dynamically reconfigurable processor arrays,". *ICFPT 2007*, pp. 273–276.